Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.078”**

**PAD FUNCTIONS:**

1. **A0**
2. **EN**
3. **V-**
4. **S1A**
5. **S2A**
6. **S3A**
7. **S4A**
8. **DA**
9. **DB**
10. **S4B**
11. **S3B**
12. **S2B**
13. **S1B**
14. **V+**
15. **GND**
16. **A1**

**3**

**4**

**5**

**6**

**2 1 16 15**

**14**

**13**

**12**

**11**

**7 8 9 10**

**.134”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V +**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .078” X .134” DATE: 10/5/21**

**MFG: MAXIM THICKNESS .016” P/N: DG409C/D**

**DG 10.1.2**

#### Rev B, 7/19/02